DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 26, 27 and 30 are rejected under 35 U.S.C. 102(b) as being anticipated by Sato (US 6,083,770).

Regarding claims 26, 30, Sato discloses a semiconductor device comprising: a semiconductor chip (10) having a rear side and a top side with contact surfaces thereon, a chip island (70) having the rear side soldered thereto with a first diffusion-soldered joint having a first melting point, flat conductors (other two layers 70) soldered to the contact surfaces on the top side of the semiconductor chip with a second diffusion soldered joint having a second melting point. See Fig.5.

Regarding claim 27, as shown in Fig.5, a metal layer (40) of Ni is between the diffusion soldered joints and the respective top side and rear side of the semiconductor chip.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 31 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sato et al. in view of Huang et al. (US 5,882,955).

Sato teaches that metal layers between the top, the rear sides and the soldered joints. However, Sato et al. does not explicitly teach that one of metal layers is a silver layer.

It is conventional and al so taught by Huang et al. that silver layer is commonly formed between the soldered joint and the surface of the chip.

It would have been obvious to one of ordinary skill in the art to provide the silver layer between the soldered joint and the surface of the chip as taught by Huang et al. in order to obtain a good bonding. See col.6 lines 27-31.

Claims 28, 33, 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sato et al. in view of Kim (US 6,774,495) and Srivastava et al. (US 6,293,457).

Sato teaches that metal layers between the top, the rear sides and the soldered joints. However, Sato et al. does not explicitly teach that the layer sequence made up of Al and Ti between the soldered joint and the surface of the chip.

It is conventional and al so taught by Kim (3G) and Sirvastava et al. (Fig.5C) that sequence layers of Al and Ti is commonly formed between the soldered joint and the surface of the chip.

It would have been obvious to one of ordinary skill in the art to provide the sequence layers of Al and Ti between the soldered joint and the surface of the chip as taught by Kim and Srivastava et al. because this arrangement of layers is well known in the art for providing good adhesive and good barrier between the soldered joint and the surface of the chip.

Claims 35 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sato et al. in view of Slater et al. (US 6,888,167).

Sato et al. teaches that soldered alloy is formed of Pb/Sn alloy (col.3 lines 55-60). However, Sato et al. does not explicitly teach the alloy such as Au/Ge and Au/Sn can be used for solder alloy.

It is conventional and also taught by Slater et al. (col.9 lines 1-2) that the alloy such as Pb/Sn, Au/Sn, and Au/Ge are art recognized materials for forming the solder alloy and they are interchangeable.

So, it would have been obvious to one or ordinary skill in the art to use Au/Sn and Au/Ge instead of Pb/Sn for the solder alloy as taught by Slater et al. It also would have been obvious to one of ordinary skill in the art to provide weight percentage of Ge and Sn in the alloy as claimed because the percentage of Sn and Ge in the solder alloy would have been determinable by one of ordinary skill in the art through no more than routine experimentation. See In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955).

Allowable Subject Matter

3. Claim 29 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

4. The following is an examiner's statement of reasons for allowance: the above combination of references does not teach the first and second solder joints having the materials as claimed in claim 29.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cuong Nguyen whose telephone number is (571) 272-1661. The examiner can normally be reached on 8:00 am to 5:30 pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Gurley can be reached on (571) 272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

7. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Cuong Q Nguyen/

Primary Examiner, Art Unit 2811

3/29/2010